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Basson et al.

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(54) **LOW LATENCY INTERCONNECT BUS PROTOCOL**

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(51) **Int. Cl.**

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G06F 13/38	(2006.01)
H04L 29/06	(2006.01)
H04W 76/02	(2009.01)

(52) **U.S. Cl.**

CPC ***G06F 13/385*** (2013.01); ***H04L 69/06*** (2013.01); ***H04W 76/02*** (2013.01)

(58) **Field of Classification Search**

USPC 370/464–477

See application file for complete search history.

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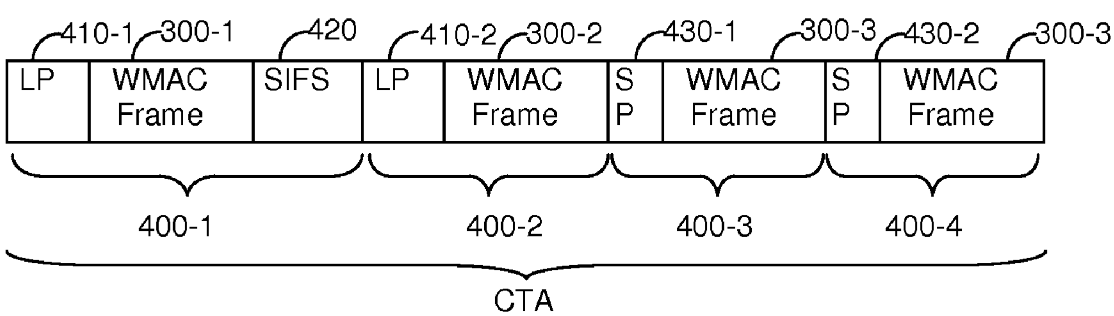
Assistant Examiner — Juvena Loo

(57) **ABSTRACT**

A method for enabling a low latency medium access control for an interconnect bus protocol over a wireless medium is provided. The method comprises constructing a wireless medium access control (WMAC) frame, wherein the WMAC frame includes a plurality of medium access control service data units (MSDUs) being aggregated according to their transmission order, the MSDUs include transaction layer packets generated by a component of the interconnect bus, wherein transmission of the WMAC frame over the wireless medium provides any one of an implied acknowledgment (ACK) mechanism and a block ACK mechanism.

15 Claims, 4 Drawing Sheets



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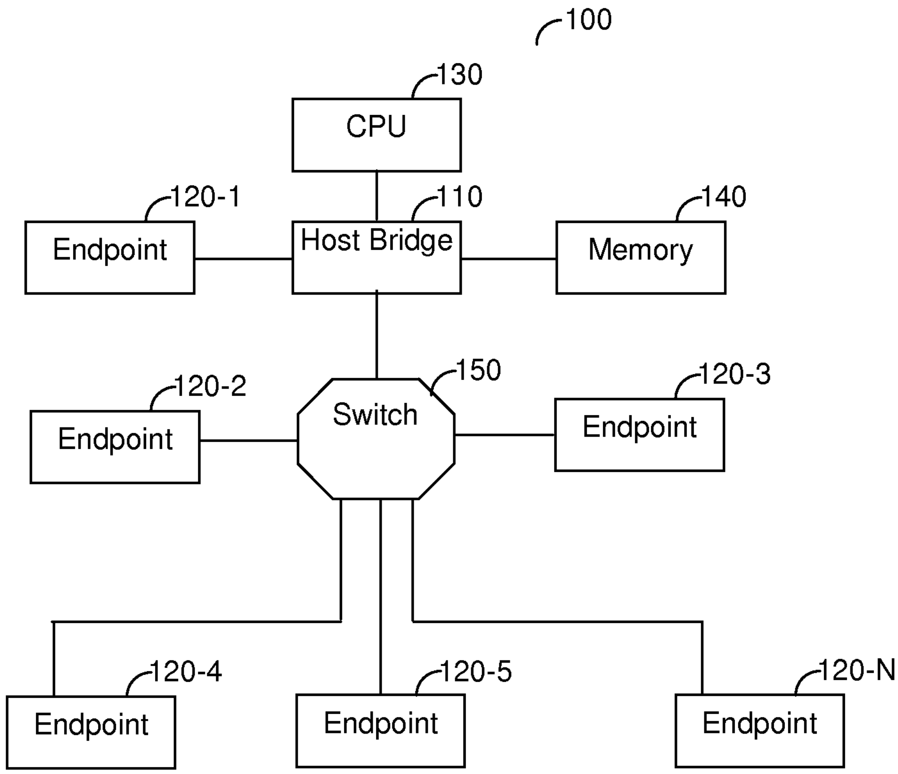
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130
CPU
120-1
Endpoint
110
Host Bridge
140
Memory
120-2
Endpoint
150
Switch
120-3
Endpoint
120-4
Endpoint
120-5
Endpoint
120-N
Endpoint

FIG. 1

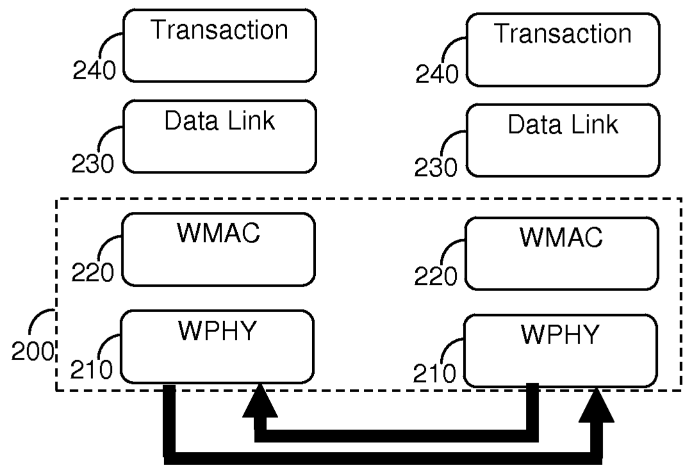

FIG. 2

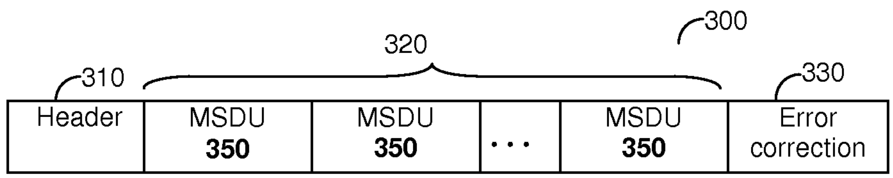

FIG. 3A

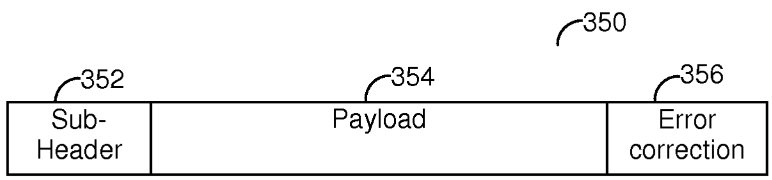

FIG. 3B

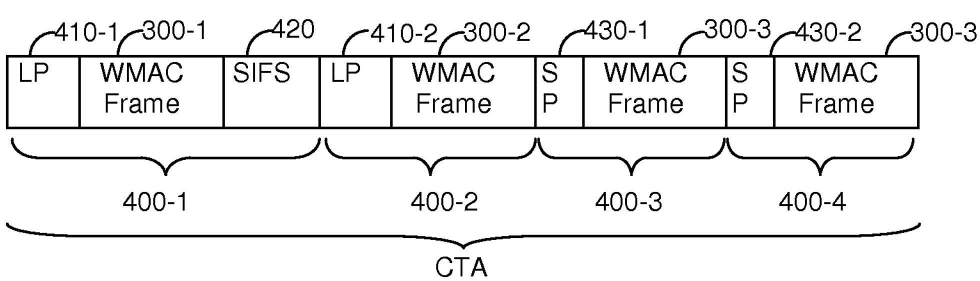

FIG. 4

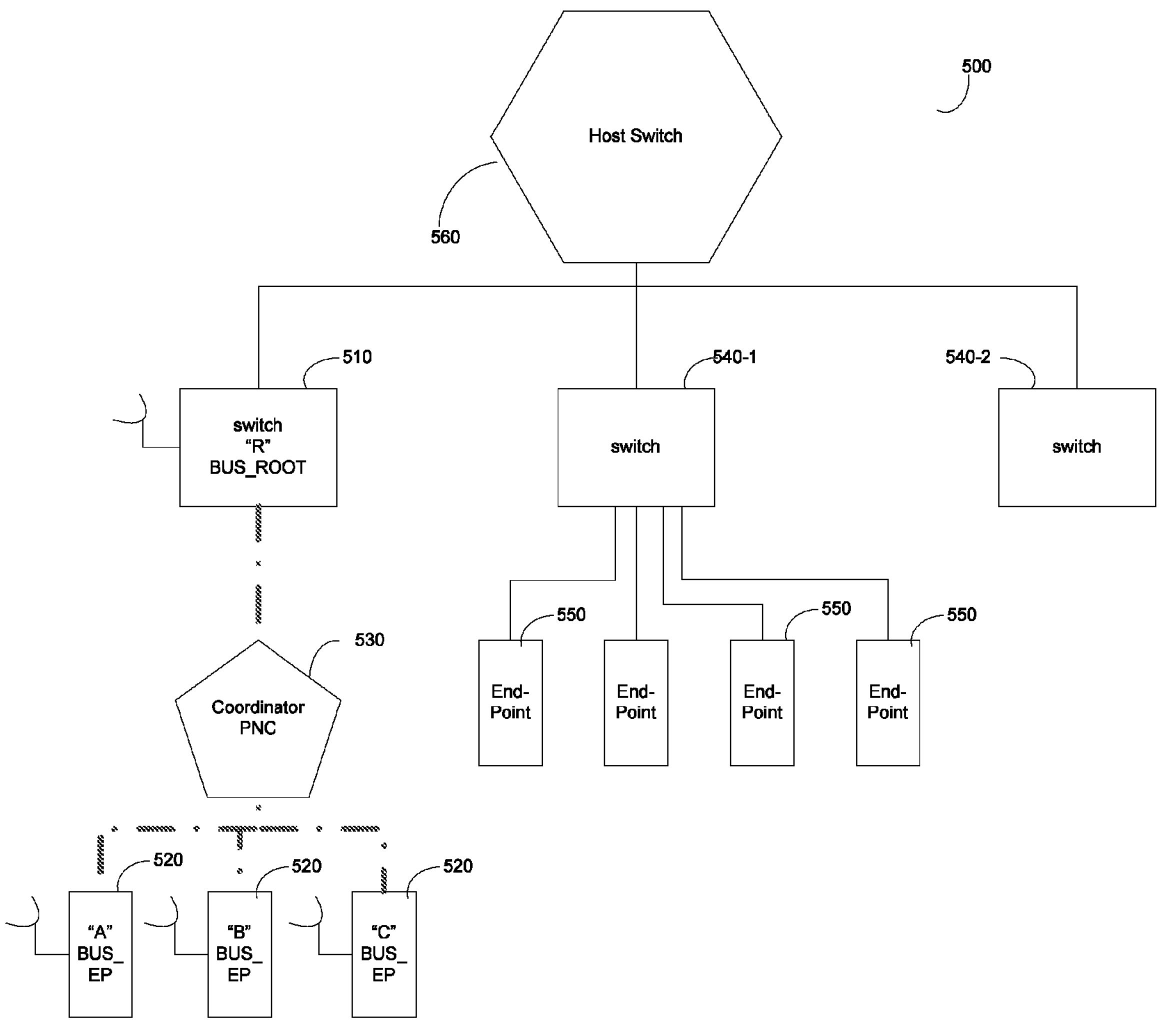
500
Host Switch
560
510
switch
"R"
BUS_ROOT
540-1
switch
540-2
switch
530
Coordinator
PNC
550
550
550
End-
Point
End-
Point
End-
Point
End-
Point
520
520
520
"A"
BUS_
EP
"B"
BUS_
EP
"C"
BUS_
EP

FIG. 5

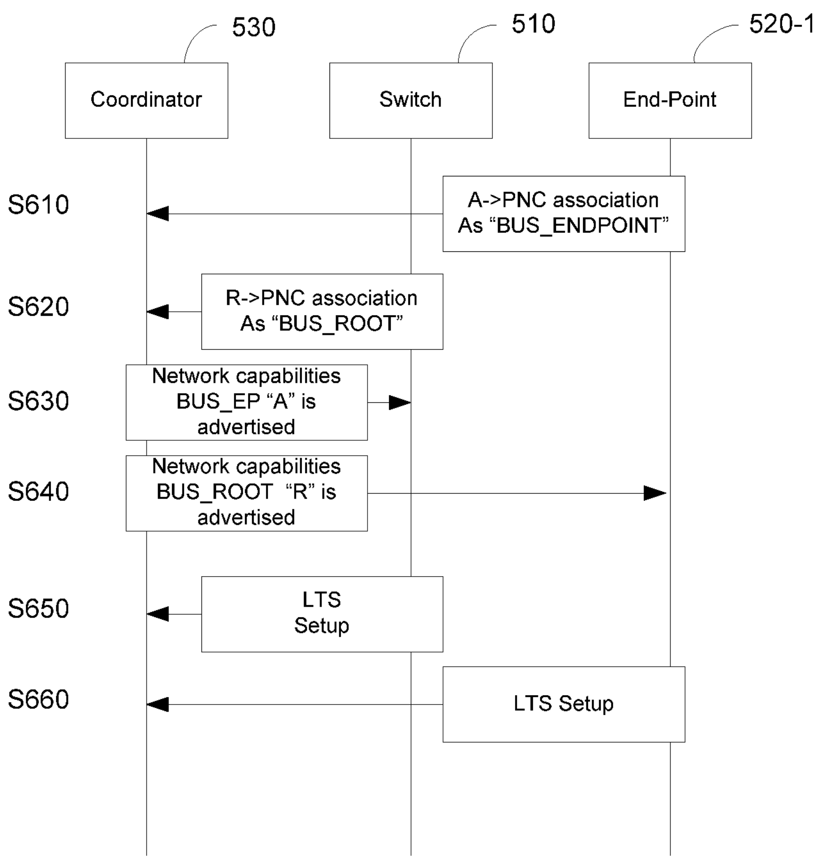
530
510
520-1
Coordinator
Switch
End-Point
S610
A->PNC association
As "BUS_ENDPOINT"
S620
R->PNC association
As "BUS_ROOT"
S630
Network capabilities
BUS_EP "A" is
advertised
S640
Network capabilities
BUS_ROOT "R" is
advertised
S650
LTS
Setup
S660
LTS Setup

FIG. 6

LOW LATENCY INTERCONNECT BUS PROTOCOL

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation application of U.S. patent application Ser. No. 12/372,009, having a filing date of Feb. 17, 2009, now issued as a U.S. Pat. No. 8,416,803. The Ser. No. 12/372,009 application claims the benefit of U.S. Provisional Application No. 61/028,879 filed on Feb. 14, 2008 and U.S. Provisional Application No. 61/091,864 filed Aug. 26, 2008, the contents of which are herein incorporated by reference.

TECHNICAL FIELD

The present invention relates generally to peripheral component interconnect buses.

BACKGROUND

Peripheral component interconnect PCI Express (or "PCIe") is a high performance, generic and scalable system interconnect bus for a wide variety of applications ranging from personal computers to embedded applications. PCIe implements a serial, full duplex, multi-lane, point-to-point interconnect, packet-based, and switch-based technology. Current versions of PCIe buses allow for a transfer rate of 2.5 Gb/Sec per lane, with a total of 32 lanes.

FIG. **1** shows an illustration of a typical architecture **100** of a computing device that includes a PCIe fabric. A host bridge **110** is coupled to endpoints **120**, a CPU **130**, a memory **140**, and a switch **150**. The peripheral components are connected through endpoints **120-1** to **120**-N (generally referred to as **120**). Multiple point-to-point connections are accomplished by the switch **150**, which provides the fanout for the I/O bus. The switch **150** provides peer-to-peer communication between different endpoints **120**. That is, traffic between the switch **150** and endpoints **120** that does not involve cache-coherent memory transfers, is not forwarded to the host bridge **110**. The switch **150** is shown as a separate logical element but it could be integrated into the host bridge **110**.

The roundtrip time of a PCIe bus is a major factor in degrading the performance of the bus. The roundtrip time is the time period elapsed from the transmission of data, for example, by the switch **150**, to the acknowledgment of the data reception by a PCIe endpoint **120**. The roundtrip time of a PCIe bus depends on the delay of a link between the switch **150** and a PCIe endpoint **120**. Typically, this delay is due to an Acknowledgment (ACK) and flow control update latencies caused by the layers of a PCIe bus.

In the abstract, the PCIe is a layered protocol bus, consisting of a transaction layer, a data link layer, and a physical layer. The data link layer waits to receive an ACK signal for transaction layer packets during a predefined time window. If an ACK signal is not received during this time window, unacknowledged packets are re-transmitted. This results in inefficient bandwidth utilization of the bus as it requires retransmission of packets with no data integrity problem. That is, a high latency between the PCIe components may cause poor bandwidth utilization.

In the current technology, peripheral devices are physically coupled to the PCIe components (e.g., endpoints, switches, etc.). In fact, these PCIe components are always connected on

the same electric board. Thus, the roundtrip time is typically very short and the PCIe is not designed to properly operate in a high latency environment.

In the related art, a few solutions have been proposed to wirelessly connect peripheral devices. These solutions are addressed to replace bus connectivity where the latency of the bus is not critical to the operation of the devices. However, connectivity of PCIe components over the air would significantly increase the latency of the link, and therefore degrade the performance of the bus.

It would be therefore advantageous to provide a solution that enables the wireless connection between all types of peripheral devices to the computing device.

SUMMARY

Certain embodiments disclosed herein include a method for enabling a low latency medium access control for an interconnect bus protocol over a wireless medium. The method comprises constructing a wireless medium access control (WMAC) frame, wherein the WMAC frame includes a plurality of medium access control service data units (MSDUs) being aggregated according to their transmission order, the MSDUs include transaction layer packets generated by a component of the interconnect bus, wherein transmission of the WMAC frame over the wireless medium provides any one of an implied acknowledgment (ACK) mechanism and a block ACK mechanism.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter that is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other features and advantages of the invention will be apparent from the following detailed description taken in conjunction with the accompanying drawings.

FIG. **1** is a block diagram showing a conventional architecture of a computer computing device;

FIG. **2** is a diagram illustrating the layers of the low latency interconnect bus protocol realized in accordance with an embodiment of the invention;

FIGS. **3**A and **3**B are respective diagrams of a WMAC frame and a MSDU constructed in accordance an embodiment of the invention;

FIG. **4** is a diagram of a WPHY frame structure constructed in accordance an embodiment of the invention;

FIG. **5** is a diagram of a wireless fabric constructed according to an embodiment of the invention; and

FIG. **6** is a diagram illustrating the process for establishing a wireless link between components connected using the low latency interconnect bus protocol in accordance with an embodiment of the invention.

DETAILED DESCRIPTION

It is important to note that the embodiments disclosed by the invention are only examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily limit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others. In general, unless otherwise indicated, singular elements may be in plural and vice versa with no loss of generality. In the drawings, like numerals refer to like parts through several views.

In accordance with certain embodiments of the invention it is provided a low latency bus protocol, a device and method that enables the connectivity of peripheral devices over a wireless medium. The low latency transmission is realized by modifying the Physical (PHY) layer and Medium Access Control (MAC) layer of a standard wireless communication protocol including, but not limited to, the protocol defined in the IEEE 802.15 standard (hereinafter the "802.15 protocol").

Generally, the 802.15 protocol refers to a family of IEEE standards dealing with communication between devices in the wireless Personal Area Network (PAN). A typical PAN includes a coordinator and one or more devices. The coordinator controls the transmission over the PAN by sending beacons to the one or more devices. The 802.15 protocol defines a mechanism that ensures collision avoidance through a Channel Time Allocation (CTA) period. That is, during a CTA period only a single device "talks" while the other paired device in the PAN "listen". The 802.15 protocol is designed to enable a Time Division Duplex (TDD) mode of operation.

The low latency interconnect bus protocol realized in accordance with an embodiment of the invention is based on a layered protocol. As illustrated in FIG. **2**, the layers of a low latency bus protocol **200** include a Wireless Physical (WPHY) layer **210** and a Wireless MAC (WMAC) layer **220**. The layer protocol **200** may also include a data link layer **230** and a transaction layer **240**. In one embodiment of the invention, the layers **230** and **240** are layers of a PCIe bus. In this embodiment, the transaction layer **240** is responsible for assembling and disassembling Transaction Layer Packets (TLPs). TLPs are used to carry transactions, where each TLP has a unique identifier that enables a response directed at the originator. The size of a typical (TLP) is relatively small (e.g., 4 Bytes to 256 Bytes). The data link **230** acts as an intermediate between the transaction layer **240** and WPHY **310**, and provides a reliable mechanism for exchanging TLPs. It should be noted that the layers **230** and **240** are not limited to PCIe layers and can be replaced by layers of any high speed serial interconnect bus that requires low latency data transfer.

The WPHY layer **210** is adapted to enable at least a bi-directional communication between components including, but not limited to, PCIe components during a single CTA. The WMAC layer **220** reduces the latency involved with sending data over a wireless medium in a TDD fashion. In addition, the WMAC layer **220** is responsible for establishing the wireless link between the components.

In accordance with one embodiment of the present invention, the WMAC layer **220** aggregates data received from the transaction layer **240** and generates a WMAC frame. An exemplary structure of an (aggregated) WMAC frame **300** is shown in FIG. **3**A. The WMAC frame **300** includes a header field **310**, a data portion **320** and an error correction field **330** with an error detection code (e.g., a CRC, a checksum, etc.) including the WMAC frame header **310**. The header **310** may include a source address, a destination address, the TDD schedule, the network capabilities, or any other type of information used for managing the wireless link. The data portion **320** includes an aggregation of a plurality of MAC Service Data Units (MSDUs) **350**.

As shown in FIG. **3**B each MSDU **350** includes a sub-header **352** a payload **354**. In some exemplary embodiments the MSDU **350** includes an error correction field **356**. The payload **354** may include one of: a data packet, such as a Transaction Layer Packet (TLP) received from the layer **240**, an idle packet or a block ACK. The error correction field **356** includes a code (e.g., a CRC code, a checksum, etc.) computed over the data in the payload **354**. The sub-header **352** may include a sequence number, a length, and a payload type (i.e., a data packet, an idle packet, or a block ACK) of the MSDU.

The aggregation of MSDUs, and thereby TLPs is essential to increase the efficiency of transmitting data over a wireless medium. As mentioned above, the size of a typical TLP is small, and therefore sending WMAC frames **300** without aggregating of TLPs significantly decreases the performance of the bus, as the overhead in transmitting a single TLP is high.

The aggregated MSDUs must be received in the same order that they were transmitted. That is, out of order MSDUs are delayed by the destination MAC, until all MSDUs are available in-order. With this aim, the WMAC layer **220** further provides a reliable link for the transaction layer **240** by implementing two mechanisms for ensuring that MSDUs sent from a source component (originated at a source WMAC layer **220**) are received with minimum latency in-order at the destination WMAC layer. These mechanisms include an implied ACK and a block ACK. To simplify the description of these mechanisms the source WMAC layer and destination WMAC layer will be referred hereinafter as layers **220-1** and **220-2** respectively.

An implied ACK is sent from the destination WMAC layer **220-2** to the source WMAC layer **220-1** and includes the sequence number of the most-recent consecutive MSDU received at the destination. For example, if a WMAC frame containing MSDUs having sequence numbers 1, 2, 3, 4, 5, 6 and 7, but the destination WMAC layer **220-2** received only MSDUs having sequence numbers 1, 2, 3, 6 and 7, in this case, the implied ACK includes the number 3 indicating that MSDUs 1, 2 and 3 received according to their order in the destination WMAC layer **220-2**. The implied ACK is sent in the WMAC frame header **310**.

The block ACK mechanism provides an indication which MSDUs were correctly received at the destination WMAC layer **220-2**, and those MSDUs that should be retransmitted by the source WMAC layer **220-1**. Specifically, the block ACK indicates the sequence number of the most-recent and non-consecutive acknowledged MSDU. In the case of the above example, the block ACK includes the number 1, 2, 3, 6 and 7 of the most recent non-consecutive acknowledged MSDU. The block ACK may be sent in a WMAC frame as a MSDU, where the number is inserted to the payload and the payload type in the sub-header is designated as a "block ACK."

The implied ACK allows the source WMAC layer **220-1** to release all consecutive MSDUs that were acknowledged (e.g., MSDUs 1, 2 and 3). All acknowledged MSDUs which were not acknowledged by the destination WMAC layer **220-2** are kept at the source WMAC layer **220-1**. Those MSDUs are retransmitted by the WMAC layer **220-1**, upon reception of a block ACK request. In accordance with an embodiment of the invention, the source WMAC layer **220-1** is required to manage a retransmission reference number which is updated to the next (new) MSDU sequence number following the retransmitted MSDU. The source WMAC layer **220-1** retransmits MSDUs having a reference-sequence number lower than the number indicated in the block ACK frame. Referring to the above example, the retransmission reference number is set to 3, the block ACK is 7, and therefore MSDUs 4 and 5 are retransmitted, since their reference number entries would be the consecutive numbers of the reference number. This mechanism allows the source WMAC layer **220-1** to avoid repeated retransmission of non-acknowledged MSDUs, thereby decreasing the latency of data retransmissions and increasing the wireless network efficiency.

In a preferred embodiment the WMAC frame **300** header field **310** contains a field which indicates the receiver's buffer size for a better flow control between the transmitter and the receiver. The header field **310** is a message sent from the receiver to the transmitter in which the receiver informs the transmitter its available buffer size. In general, the transmitter should consider the receiver's buffer size and not transmit more than the receiver capacity as indicated by the buffer size. The indication from the receiver to the transmitter is per Block ACK, therefore it is dynamic and can accommodate dynamic changes in the receiver buffer size.

The WPHY layer **210** receives the WMAC frame **300** and constructs one or more WPHY frames **400**, such as shown in FIG. **4** (e.g. **400-1**, **400-2**, **400-3**, **400-4**). The frame **400** allows the bi-directional communication between two PCIe components during a single CTA. The frame **400** may be constructed to include a long preamble **410**, a Short Inter-Frame Space (SIFS) field **420**, a short preamble (SP) **430**, and a WMAC frame **300**.

The long preamble field **410** is a predefined sequence utilized for signal detection, energy measurements, time, frequency and phase synchronization, channel estimation, antenna steering, calibrations, frame delimiters, etc. The short preamble **430** may be used for fast channel estimation, channel acquisition, frequency and time errors estimation, etc. The WMAC frame **300** can be sent either by the source layer **220-1** or the destination layer **220-2**.

The content of the WPHY frame **400** is determined according to the communication state between two communicating components. Specifically, a long preamble **410** is included in a WPHY frame **400** at the first time that a WMAC frame **400** is sent. When the two components exchange the long preamble **410**, the switching between WMAC frames **300** is performed using short preambles **430**. It should be noted that the size of the long preamble is longer than the short preamble.

In the example shown in FIG. **4**, during a single CTA, four WPHY frames **400-1** through **400-4** are transferred between two components A and B. The first frame **400-1** is sent from the component-A and includes a long preamble **410-1**, a SIFS **420** and a WMAC frame **300-1**. The second frame **400-2** is the first frame sent from the component-B and also includes a long preamble **410-2** and a WMAC frame **300-2**. A third frame **400-3** is sent from the component-A and includes a short preamble **430-1** and a WMAC frame **300-3**. A forth frame **400-4** is sent from the component-B and includes a short preamble and a WMAC frame **300-4**. The inter frame spacing of the frames **400-3** and **400-4** is shorter than SIFS **420**.

In accordance with one embodiment of the invention the low latency interconnect bus protocol **200** can be utilized in a computing device to wirelessly connect a plurality of peripheral components to the device. The computing device may be, but is not limited to, a personal computer, a laptop, a media player, a mobile phone, a personal digital assistant (PDA), and the likes. FIG. **5** is a block diagram of a fabric **500** used for enabling wireless connectivity between peripheral components using the low latency interconnect bus protocol **200**.

In accordance with one embodiment of the invention a switch **510** communicates with a plurality of endpoints **520**, over a wireless medium, through a coordinator **530**. The switch **510** and endpoints **520** implement the layer protocol **200** and are compliant with at least the PCIe specification. The switches **540-1** and **540-2** and the endpoints **550** are standard PCIe components. A host switch **560** identifies the switch **510** and endpoints **520** as standard PCIe components. Therefore, data is transferred between the switch **510** and endpoints **520**, where the underlying wireless specifics are transparent to any component connected to the fabric **500**.

In order to transfer data between the switch **510** and endpoints **520**, firstly, a wireless link should be established between these components. The process for establishing the wireless link is described in FIG. **6**. At S**610**, the endpoint **520-1** sends an association request to the coordinator **530**. At S**620**, the switch **510** also sends an association request to the coordinator **530**. At S**630**, the coordinator **530** transmits its network capabilities to the switch **510** and subsequently, at S**640**, the network capabilities are also advertised to the endpoint **520-1**. Thereafter, at S**650**, a request to setup a Link Transmission Slot (LTS) is sent from the switch **510** to the coordinator **530**. At S**660**, a LTS setup request is sent from the endpoint **520-1** to the coordinator **530**. Upon reception of the LTS setup requests a wireless link is established between the end-point **520-1**, the switch **510** and the coordinator **530**.

The invention has now been described with reference to specific embodiments where the low latency interconnect bus protocol is utilized to enable the connectivity of peripheral devices connected to PCIe components. Other embodiments will be apparent to those of ordinary skill in the art. For example, the low latency interconnect bus protocol can be adapted for the use with peripheral devices utilizing connection formats, such as PCIe second generation, PCIe third generation, USB, SATA, HyperTransport, Infiniband, serial and fast point-to-point interconnects, and the like.

The teachings of the invention described may be implemented in hardware, firmware, software or any combination therefore. In an embodiment of the present invention, some or all of the processes and components are implemented as a computer executable code. Such a computer executable code contains a plurality of computer instructions that when performed result with the execution of the tasks disclosed herein. Such computer executable code may be available as source code or in object code, and may be further comprised as part of, for example, a portable memory device or downloaded from the Internet, or embodied on a program storage unit or computer readable medium. The principles of the present invention may be implemented as a combination of hardware and software and because some of the constituent system components and methods depicted in the accompanying drawings may be implemented in software, the actual connections between the system components or the process function blocks may differ depending upon the manner in which the present invention is programmed.

The computer executable code may be uploaded to, and executed by, a machine comprising any suitable architecture. Preferably, the machine is implemented on a computer platform having hardware such as one or more central processing units ("CPUs"), a random access memory ("RAM"), and input/output interfaces. The computer platform may also include an operating system and microinstruction code. The various processes and functions described herein may be either part of the microinstruction code or part of the application program, or any combination thereof, which may be executed by a CPU, whether or not such computer or processor is explicitly shown. In addition, various other peripheral units may be connected to the computer platform such as an additional data storage unit and a printing unit. Explicit use of the term CPU, "processor" or "controller" should not be construed to refer exclusively to hardware capable of executing software, and may implicitly include, without limitation, digital signal processor hardware, ROM, RAM, and non-volatile storage.

All examples and conditional language recited herein are intended for pedagogical purposes to aid the reader in understanding the principles of the invention and the concepts contributed by the inventor to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions. Moreover, all statements herein reciting principles, aspects, and embodiments of the invention, as well as specific examples thereof, are intended to encompass both structural and functional equivalents thereof. Additionally, it is intended that such equivalents include both currently known equivalents as well as equivalents developed in the future, i.e., any elements developed that perform the same function, regardless of structure.

What is claimed is:

1. A method for enabling a medium access control for an interconnect bus over a wireless medium, comprising:

constructing a wireless medium access control (WMAC) frame, wherein the WMAC frame includes a plurality of medium access control service data units (MSDUs) being aggregated according to their transmission order, the MSDUs include transaction layer packets generated by a component of the interconnect bus;

transmitting the WMAC frame over the wireless medium wherein transmission of the WMAC frame provides an implied acknowledgment (ACK) mechanism or a block ACK mechanism, wherein the implied ACK mechanism is implemented by including, in the WMAC frame, a sequence number of a most-recent consecutive MSDU received, and wherein the block ACK mechanism is implemented by including, in the WMAC frame, a sequence number of a most-recent and non-consecutive acknowledged MSDU.

2. The method of claim **1**, further comprising encapsulating the WMAC frame in a wireless physical (WPHY) frame, wherein the transmitting comprises transmitting the wireless physical (WPHY) frame.

3. The method of claim **1**, wherein the WMAC frame further comprises:

a header field constructed to maintain at least an indication of a buffer size of a receiver for enabling a flow control between a transmitter and the receiver; and

an error correction field including an error detection code computed based on a data portion of the WMAC frame and the header field.

4. The method of claim **1**, wherein the WMAC frame further comprises: a data portion constructed to maintain the aggregation of the plurality of MSDUs.

5. The method of claim **1**, wherein each MSDU comprises:

a sub-header constructed to maintain at least a length field; and

a payload constructed to maintain a data packet, an idle packet, or a block ACK.

6. The method of claim **1**, wherein the interconnect bus is a wireless peripheral component interconnect (PCI) express bus.

7. The method of claim **6**, wherein the PCI express bus comprises at least one of a switch, an endpoint, or a coordinator.

8. A non-transient computer readable medium for enabling a medium access control for an interconnect bus over a wireless medium having instructions stored thereon for:

constructing a wireless medium access control (WMAC) frame, wherein the WMAC frame includes a plurality of medium access control service data units (MSDUS) being aggregated according to their transmission order, the MSDUs include transaction layer packets generated by a component of the interconnect bus; and

transmitting the WMAC frame over the wireless medium, wherein transmission of the WMAC frame provides an implied acknowledgment (ACK) mechanism or a block ACK mechanism, wherein the implied ACK mechanism is implemented by including, in the WMAC frame, a sequence number of a most-recent consecutive MSDU received, and wherein the block ACK mechanism is implemented by including, in the WMAC frame, a sequence number of a most-recent and non-consecutive acknowledged MSDU.

9. An apparatus for enabling a medium access control for an interconnect bus over a wireless medium, comprising:

at least one processor configured to construct a wireless medium access control (WMAC) frame, wherein the WMAC frame includes a plurality of medium access control service data units (MSDUs) being aggregated according to their transmission order, the MSDUs include transaction layer packets generated by a component of the interconnect bus; and

a transmitter configured to transmite the WMAC frame over the wireless medium wherein transmission of the WMAC frame provides an implied acknowledgment (ACK) mechanism or a block ACK mechanism, wherin the implied ACK mechanism is implemented by including, in the WMAC frame, a sequence number of a most-recent consecutive MSDU received, and wherein the block ACK mechanism is implemented by including, in the WMAC frame, a sequence number of a most-recent and non-consecutive acknowledged MSDU.

10. The apparatus of claim **9**, wherein the interconnect bus is a wireless peripheral component interconnect (PCI) express bus.

11. The apparatus of claim **10**, wherein the PCI express bus comprises at least one of a switch, an endpoint, or a coordinator.

12. The apparatus of claim **9**, wherein the transmitted WMAC frame is encapsulated in a wireless physical (WPHY) frame.

13. The apparatus of claim **9**, wherein the WMAC frame further comprises:

a header field constructed to maintain at least an indication of a buffer size of a receiver for enabling a flow control between a transmitter and the receiver; and

an error correction field including an error detection code computed based on a data portion of the WMAC frame and the header field.

14. The apparatus of claim **9**, wherein the WMAC frame further comprises a data portion constructed to maintain the aggregation of the plurality of MSDUs.

15. The apparatus of claim **9**, wherein each MSDU comprises a sub-header constructed to maintain at least a length field and a payload constructed to maintain a data packet, an idle packet, or a block ACK.

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